WHAT IS CLAIMED IS:

1. A booster circuit comprising:

a boosting section including one or a plurality of serially-connected boosting cells for boosting an input voltage in response to a clock signal and outputting the boosted voltage, each of the boosting cells including a charge transfer transistor and a plurality of boosting capacitors connected in parallel;

a boosted voltage detector for detecting the boosted voltage output from the boosting section and, when the detected boosted voltage is lower than or equal to a given voltage value, outputting a detection signal; and

a clock generator for outputting the clock signal in response to the detection signal,

wherein the boosting section includes a connection switching circuit for switching connections to the plurality of boosting capacitors based on the control signal.

2. The booster circuit of claim 1, further comprising a boosted voltage detection control section for detecting the output voltage from the boosting section and outputting the control signal.

3. The booster circuit of claim 2, further comprising a power supply voltage detection control section for detecting a power supply voltage and controlling the output of the boosted voltage detection control section.

4. The booster circuit of claim 1, further comprising a boosted voltage detection control section for detecting a power supply voltage and outputting the control signal.

5. A booster circuit comprising:

a clock amplitude switching section for changing the amplitude of a first clock signal to switch to a second clock signal and outputting the second clock signal, based on a control signal;

a boosting section including one or a plurality of serially-connected boosting cells for boosting an input voltage in response to the second clock signal and outputting the boosted voltage, each of the boosting cells including a charge transfer transistor and a boosting capacitor;

a boosted voltage detector for detecting the boosted voltage output from the boosting section and, when the detected boosted voltage is lower than or equal to a given voltage value, outputting a detection signal; and

a clock generator for outputting the first clock signal in response to the detection signal.

6. The booster circuit of claim 5, further comprising a boosted voltage detection control section for detecting the output voltage from the boosting section and outputting the control signal.

7. The booster circuit of claim 6, further comprising a power supply voltage detection control section for detecting a power supply voltage and controlling the output of the boosted voltage detection control section.

8. The booster circuit of claim 5, further comprising a boosted voltage detection control section for detecting a power supply voltage and outputting the control signal.

9. A booster circuit comprising:

a boosting section including one or a plurality of serially-connected boosting cells,

each of the boosting cells including

a plurality of charge transfer transistors connected in parallel, each receiving an output voltage from one of the transistors at a previous stage and outputting the received voltage to one of the transistors at a subsequent stage and

an output-voltage capacitor having an electrode connected to output terminals of the charge transfer transistors and another electrode to which a first clock signal is input;

a boosted voltage detector for detecting the boosted voltage output from the boosting section and, when the detected boosted voltage is lower than or equal to a given voltage value, outputting a detection signal; and

a clock generator for outputting the first clock signal and a second clock signal having a phase different from that of the first clock signal, in response to the detection signal,

wherein the boosting section includes

a plurality of gate boosting capacitors each having an electrode connected to a gate of an associated one of the charge transfer transistors and another electrode to which the second clock signal is input,

a charge-transfer-transistor control circuit connected to the gate boosting capacitors and used for selectively operating the charge transfer transistors based on the control signal, and

a plurality of switching transistors for establishing an electrical connection or disconnection between an input terminal and a gate of each of the charge transfer transistors.

10. The booster circuit of claim 9, further comprising a boosted voltage detection control section for detecting the output voltage from the boosting section and outputting the control signal.

11. The booster circuit of claim 10, further comprising a power supply voltage detection control section for detecting a power supply voltage and controlling the output of the boosted voltage detection control section.

12. The booster circuit of claim 9, further comprising a boosted voltage detection control section for detecting a power supply voltage and outputting the control signal.

13. A booster circuit comprising:

a boosting section including one or a plurality of serially-connected boosting cells,

each of the boosting cells including

a plurality of charge transfer transistors connected in parallel, each receiving an output voltage from one of the transistors at a previous stage and outputting the received voltage to one of the transistors at a subsequent stage and

an output-voltage capacitor having an electrode connected to output terminals of the charge transfer transistors and another electrode to which a first clock signal is input;

a boosted voltage detector for detecting the boosted voltage output from the boosting section and, when the detected boosted voltage is lower than or equal to a given voltage value, outputting a detection signal; and

a clock generator for outputting the first clock signal and a second clock signal having a phase different from that of the first clock signal, in response to the detection signal,

wherein the boosting section includes

a plurality of gate boosting capacitors each having an electrode connected to a gate of an associated one of the charge transfer transistors and another electrode to which the second clock signal is input,

a charge-transfer-transistor shift control circuit connected to the gate boosting capacitors and used for operating the charge transfer transistors with the number of operating transistors changed, and

a plurality of switching transistors for establishing an electrical connection or disconnection between an input terminal and a gate of each of the charge transfer transistors.